CLAIMS

What is claimed is:

1. A cache coherent multiple processor integrated circuit, comprising:

a plurality of processor units;

a plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded RAM unit for storing instructions and data for the processor units;

a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

2. The circuit of Claim 1, further comprising an input output unit coupled to the bus to provide input and output transactions for the processor units.

3. The circuit of Claim 1, wherein the bus is configured to provide split transactions for the processor units coupled to the bus.

4. The circuit of Claim 1, wherein the bus is configured to transfer an entire cache line for the cache units of the processor units.

5. The circuit of Claim 1, wherein the bus is 256 bits wide.

6. The circuit of Claim 1, wherein the RAM unit is an embedded DRAM core.

7. The circuit of Claim 1, wherein the bus is configured to support a symmetric multiprocessing method for the plurality of processor units.

8. The circuit of Claim 1, wherein the processor units are compatible with a version of a MIPS processor core.

9. The circuit of Claim 1, wherein the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit.

10. An integrated circuit device, comprising:

an integrated circuit die; and

a power supply coupled to the integrated circuit die, wherein the integrated circuit die includes therein:

a plurality of processor units;

a plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded RAM unit for storing instructions and data for the processor units;

a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processor units and the embedded RAM unit.

11. The circuit of Claim 10, further comprising an input output unit coupled to the bus to provide input and output transactions for the processor units.

12. The circuit of Claim 10, wherein the bus is configured to provide split transactions for the processor units coupled to the bus.

13. The circuit of Claim 10, wherein the bus is configured to transfer an entire cache line for the cache units of the processor units.

14. The circuit of Claim 10, wherein the bus is 256 bits wide.

15. The circuit of Claim 10, wherein the RAM unit is an embedded DRAM core.

16. The circuit of Claim 10, wherein the bus is configured to support a symmetric multiprocessing method for the plurality of processor units.

17. The circuit of Claim 10, wherein the processor units are compatible with a version of a MIPS processor core.

18. The circuit of Claim 10, wherein the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit.

19. A portable hand-held electronic device, comprising:

an integrated circuit die; and

a power supply coupled to the integrated circuit die, wherein the integrated circuit die includes therein:

a plurality of processor units;

a plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded DRAM core unit for storing instructions and data for the processor units;

a 256 bit cache coherent bus coupled to the processor units and the embedded DRAM core unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processor units and the embedded DRAM core unit.

20. The circuit of Claim 19, wherein the bus is configured to provide split transactions for the processor units coupled to the bus.